What is Claimed is:

[c1] A multilayer semiconductor device, comprising:

a metal-insulator-metal (MIM) capacitor including a first metal plate, a dielectric layer, and a second metal plate;

a nitride etchstop layer formed above the MIM capacitor;

a first interlayer dielectric formed on the nitride etchstop layer; and

a first via and a second via that extend through at least the first interlayer dielectric to contact the nitride etchstop layer.

[c2] The multilayer semiconductor device of claim 1, wherein the nitride etchstop layer is deposited directly upon the MIM capacitor.

[c3] The multilayer semiconductor device of claim 1, wherein the first metal plate and the second metal plate correspond to a bottom plate and a top plate of the MIM capacitor, respectively.

[c4] The multilayer semiconductor device of claim 3, further comprising a second interlayer dielectric formed between the top plate and the nitride etchstop layer.

[c5] The multilayer semiconductor device of claim 4, wherein the second interlayer dielectric comprises a thickness of about 1500 Ã... to about 10,000 Ã....

[c6] The multilayer semiconductor device of claim 1, wherein the thickness of the nitride etchstop layer is about 500 Ã... to about 1500 Ã....

[c7] The multilayer semiconductor device of claim 6, wherein a thickness of the nitride etchstop layer is about 700 Ã... to about 1200 Ã....

[c8] The multilayer semiconductor device of claim 1, further comprising a wiring level that is electrically connected to at least one of the first metal plate and the second metal plate.

[c9] A method of fabricating a multilayer semiconductor device, comprising:

forming an metal-insulator-metal (MIM) capacitor including a first metal plate, a dielectric layer formed on the first metal plate, and a second metal plate formed on the dielectric layer;

patterning the second metal plate;

depositing a nitride etchstop layer above the MIM capacitor;

forming an interlayer dielectric on the nitride etchstop layer;

forming a first via and a second via through at least the interlayer dielectric by an anisotropic etch process to contact the nitride etchstop layer above the patterned second metal plate and above the first metal plate, respectively; and

removing portions of the nitride etchstop layer, where the first via and the second via contact the nitride etchstop layer.

[c10] The method of claim 9, wherein patterning the second metal plate is accomplished by an anisotropic etch process.

[c11] The method of claim 9, wherein removing portions of the nitride etchstop layer is accomplished by a selective via etch chemistry that includes any of the group of argon, nitrogen, C_4F_8 and argon or oxygen, and carbon monoxide.

[c12] The method of claim 9, wherein the depositing of the nitride etchstop layer is directly upon the MIM capacitor.

[c13] The method of claim 9, further comprising patterning at least one of the first metal plate and the dielectric layer by an anisotropic etch process.

[c14] The method of claim 13, further comprising patterning a wiring level in electrical contact with at least one of the first metal plate and the second metal plate by an anisotropic etch process.

[c15] The method of claim 9, further comprising forming a second interlayer dielectric between the second metal plate and the nitride etchstop layer.

[c16] A method of fabricating a multilayer semiconductor device including a metal-insulator-metal (MIM) capacitor, comprising:

patterning a metal top plate of the MIM capacitor by an anisotropic etch process;

depositing a nitride etchstop layer above the MIM capacitor;

forming an interlayer dielectric on the nitride etchstop layer; and

forming a first via through the interlayer dielectric by an anisotropic etch process to contact the nitride etchstop layer.

[c17] The method of claim 16, further comprising removing a first portion of the nitride etchstop layer above the MIM capacitor, so that, the first via contacts the metal top plate.

[c18] The method of claim 17, further comprising: forming a second via through the interlayer dielectric by an anisotropic etch process to contact the nitride etchstop layer.

[c19] The method of claim 18, further comprising removing a second portion of the nitride etchstop layer above the MIM capacitor, so that, the second via contacts a metal bottom plate of the MIM capacitor.

[c20] The method of claim 16, further comprising forming a second interlayer dielectric between the metal top plate and the nitride etchstop layer.